Davide Conficconi

Curriculum Vitae

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HIGHLIGHTS

- Assistant Professor (RTDA) in Information Processing Systems, Politecnico di Milano, since March 2024.
- Italian Scientific National Habilitation for Associate Professor, SSD/GSD: IINF-05/A; ING-INF/05; Information Processing Systems (equivalent to Computer Systems); 19 November 2024
- **Research Activities**
  - Co-Author of 12 Journal Papers, 9 out of 12 are Q1, in IEEE TPDS, ACM TRETS, ACM Computing Surveys, IEEE TETC, JPDC, and IEEE JBHI.
    Top Conference Publications: DAC, CGO, FPGA, ICCD
    In total: 12 Journal papers, 27 conference papers, and 1 book chapter.
  - H-index: 10; Total citations: 257 (Google Scholar, January 2025); H-index: 8; Total citations: 162 (Scopus, January 2025)
  - Research intern at *international* institutions: IBM Research Zurich 2021-22, Xilinx (now AMD) Research Dublin 2018-19.
  - *WP leader* in the GUIDO ERC PoC project; *Task leader* in the EVEREST European Project
  - Part of National Centre for HPC, Big Data and Quantum Computing (HPC)
- **Awards**
  - Different research works awarded with Artifacts Badges for reproducible research
  - (Co-)Supervisor of winner teams for an international FPGA-based design contest 24-23-22
  - best Ph.D. Intern presentation at IBM department symposium, first prize for the intern competition at Xilinx Dublin
  - First place in the IEEE Lance Stafford Larson award, and best poster award at RAW'24.
  - Interdisciplinary PhD scholarship funds for Space and Information Systems at Polimi
  - Selected to represent Polimi at the European Talent Academy 2025
- **Community Service**
  - Program Chair of RAW'25; Artifact Evaluation (AE) Chair of RAW'24, RAW'23
  - Program Committee FCCM'25-24, FPL'25-24, HPCC'24, PACRIM'24, HEART'24, SAC'24, ISPA '23, GLSVLSI'23
  - Artifact Evaluation (AE) Committee ASPLOS'25, '23, '22, CGO '25, '24, '23, MICRO'23, PLDI'23
  - Guest Editor of a Special Issue on "Secure and Efficient Distributed Computation for Emerging Systems on the Edge" (SUNRISE) on Elsevier Journal of Parallel and Distributed Computing (JPDC) 2023-2024
  - Journal (25+ manuscripts) and conferences (25+ manuscripts) reviewer for several venues
  - Volunteering for the IEEE Larson Award
- **Communication Skills**
  - Presenting the research work at FPGA'21, RAW'23-21-18, and H^{2}RC, EUROCON,
  - Presenting at international companies, e.g., Xilinx (now AMD) and IBM, and universities, e.g., Berkeley and Northeastern.
  - Presenting the internship work at intern competitions and winning the best presentation award.
- **Teaching and Advising Activities**
  - Instructor of Polimi courses among which Spring'23, Master "*Advanced Computer Architecture*" (200 students, 5 CFU)
  - Advisor of 1 PhD student, 3 Master thesis, and Co-Advisor of 3 Master thesis; supervisor of 35+ msc and bsc research projects.
  - Organizing committee and Instructor of the International CPS Summer School 2023.
  - Instructor of the *"Hardware and Accelerators: FPGAs for AI"* for Cefriel, and the *"Creative Lab"* at the CPS Summer School.
  - Teaching assistant for different courses in the field of digital design and computer architectures from 2019.

CONTENTS

SHORT BIO

Davide is an Assistant Professor (RTDA) of Information Processing Systems at Politecnico di Milano where he got his Ph.D. in Information Technology (Feb '22). His research interests is to build and codesign of Domain-Specific Computer Systems focusing on heterogeneous and reconfigurable architectures, design methodologies, computer architectures, design automation, and abstraction layers.

RESEARCH INTEREST

My research interests fall in the broad spectrum of *system architecture* field where achieving high-performance and energy-efficiency is paramount. Specifically major topics are **codesign of domain-specific systems**, architectures or frameworks that span the **system stack** (from the HDL design to the design automation, from the abstraction layer the compilation framework), **reconfigurable architectures**, especially FPGAs, **heterogeneous systems**, **design automation**, **neuromorphic computing systems**, and accelerators in general.
My codesign research interest pushed me to participate in interdisciplinary research fields where system architectures meet biomedical image processing and space systems.

SCIENTIFIC NATIONAL HABILITATION

Type of habilitation	Country	SSD/GSD/topic area	Date of achievement
Associate Professor	Italy	IINF-05/A; ING-INF/05; Information Processing Systems	19 November 2024

EDUCATION

2018 – 17 FEB. 2022 **Doctor of Philosophy** Information Technology *Politecnico di Milano*
Area: Computer Engineering
Dissertation Title: "*On the Role of Reconfigurable Systems in Domain-Specific Computing*"
Advisor: M. D. Santambrogio

2015 – 2018 **Master of Science** WITH HONORS Computer Science and Engineering *Politecnico di Milano*
Co-Author: A. Comodi
Thesis Title: "*TiReX: Tiled Regular eXpressions matching architecture*"
Advisor: M. D. Santambrogio, Co-Advisor: A. Scolari

2012 – 2015 **Bachelor of Science** Computer and Engineering *Politecnico di Milano*

RESEARCH EXPERIENCE

Politecnico di Milano CURRENT FROM MAR 2024 (MILAN)
Assistant Professor (Untenured Track):
Starting from March 2024, I am an assistant professor (untenured track) (Ricercatore a Tempo Determinato di Tipo A) in Information Processing Systems, working in the research field of (co-)designing of Domain-Specific Systems and Architectures for computations spanning from the embedded to the high-performance computing fields.
According to Italian Law: Settore Scientifico Disciplinare: IINF-05/A (Sistemi di Elaborazione delle Informazioni), Gruppo Scientifico Disciplinare: 09/IINF-05 (Sistemi di elaborazione delle informazioni).

Politecnico di Milano MAR 2022 – FEB 2024 (MILAN)
Post-Doctoral Researcher:
Carried on my research domain-specific architectures and design automation toolchains for reconfigurable computing systems. Moving also part of my research efforts on quantum computing technologies spanning from efficient and accelerated computations to design automation. Working with M. Santambrogio on managing the research efforts in the system architecture area of the NECSTLab.

IBM Research SEPT 2021 – FEB 2022 (ZURICH)
Research Intern:
Working with M.Lantz's group with D. Diamantopoulos on the cloudFPGA system. Mainly contributing to the cFp_Zoo a set of

domain-specific accelerators for the hybrid multi-cloud era, and smaller contribution to the cFDK.

Xilinx Research (now AMD) AUG 2018 – FEB 2019 (DUBLIN)
Research Intern:
Working with M. Blott's group with Y. Umuroglu. Contribution to the bit serial inference accelerator BISMO (ACM TRETS'19) and FPGA-tidbits components, both open sourced on github.

UniCredit JAN 2018 – JUL 2018 (MILAN)
Research Intern:
Collaborating with UniCredit's R&D department on a financial application targeting FPGAs, under the supervision of M. Paris.

Oracle Labs JAN 2018 – JUN 2018 (REMOTE - ZURICH)
Research Assistant:
Working as Research Assistant remotely at Oracle Labs under the supervision of D. B. Bartolini on Graph and Data visualization applications.

TEACHING ACTIVITIES

Politecnico di Milano SEPTEMBER 2024 – SEPTEMBER 2025
Instructor:
Instructor for Bachelor Course of *"Informatica Applicata"*, applied CS for data visualization, for Communication Design Bachelor Degree with 58 students. Credits: 5 CFU. Course Evaluation: n.a. .

Politecnico di Milano SEPTEMBER 2023 – SEPTEMBER 2024
Contract Professor:
Instructor for Bachelor Course of *"Informatica Applicata"*, applied CS for data visualization, for Communication Design Bachelor Degree with 70 students. Credits: 5 CFU. Course Evaluation: 2.4/4 .

CPS Summer School MAY 2023 – SEPTEMBER 2023
Organizing Committe and Instructor:
Member of the Organizing Committee and Instructor of the Creative Lab of the Cyber-Physical Systems (CPS) Summer School held in Alghero (ITA).

Politecnico di Milano FEBRUARY 2023 – JANUARY 2024
Contract Professor:
Instructor for Master Course of *"Advanced Computer Architectures"* for Computer Science and Engineering Master Degree with 231 students. Credits: 5 CFU. Course Evaluation: 3.2/4.

Politecnico di Milano FEBRUARY 2023 – JANUARY 2024
Contract Professor:
Instructor for Bachelor Course of *"Informatica e Elementi Di Informatica Medica"*, equivalent to CS101 in C, for Bionegineering Bachelor Degree with 191 students. Credits: 7 CFU. Course Evaluation: 2.6/4.

Passion in Action – Politecnico di Milano OCTOBER 2022 – FEBRUARY 2024
Instructor:
Instructor for for four editions (spring '24, fall'23, spring '23, fall'22). Course of *"FPGA101"* which introduces the Field-Programmable Gate Arrays technology along with primary design flows and system design methodologies.

CPS Summer School JULY 2022 – SEPTEMBER 2022
Creative Lab Instructor:
Instructor of the Creative Lab of the Cyber-Physical Systems (CS) Summer School held in Pula (ITA). Lab director M. D. Santambrogio.

Politecnico di Milano – CEFRIEL JULY 2022 – JULY 2022
Instructor:
Course of *"Hardware and Accelerators: FPGAs for AI"* part of the "Artificial Intelligence And Machine Learning Applications" Specialization degree ("Master universitario di primo livello")

Passion in Action – Politecnico di Milano FEB 2022 – JUNE 2022
Lecturer and Tutor:
Course of *"FPGA Academy"* held by Prof Marco D. Santambrogio

Passion in Action – Politecnico di Milano OCT 2020 – JUNE 2021
Lecturer and Tutor:
Course of *"FPGA Academy"* held by Prof Marco D. Santambrogio

Passion in Action – Politecnico di Milano FEB 2020 – JUNE 2020

Lecturer and Tutor:
Course of *"FPGA Academy"* held by Prof Marco D. Santambrogio

OTHER TEACHING ACTIVITIES

Politecnico di Milano FEB 2024 – JUNE 2024
Teaching Assistant:
Master Course of *"Advanced Computer Architectures"* held by Prof Christian Pilato with around 243 Students. Credits: 5 CFU. Course Evaluation: 3.0/4

Politecnico di Milano FEB 2023 – JUNE 2023
Teaching Assistant:
Master Course of *"Advanced Computer Architectures"* held by myself with 231 Students. Credits: 5 CFU. Course Evaluation: 3.2/4

Politecnico di Milano FEB 2022 – JUNE 2022
Teaching Assistant:
Master Course of *"Advanced Computer Architectures"* held by Prof Donatella Sciuto with 181 Students. Credits: 5 CFU. Course Evaluation: 3.1/4

Politecnico di Milano FEB 2021 – JUNE 2021
Teaching Assistant:
Master Course of *"Advanced Computer Architectures"* held by Prof Marco D. Santambrogio with 251 Students. Credits: 5 CFU. Course Evaluation: 3.3/4

Politecnico di Milano FEB 2020 – JUNE 2020
Teaching Assistant:
Master Course of *"Advanced Computer Architectures"* held by Prof Marco D. Santambrogio with 222 Students. Credits: 5 CFU. Course Evaluation: 2.7/4

MAR 2020 – APR 202
Volunteering Assistant:
Volunteering to assist online teaching and online Polimi degrees during first Covid-19 lockdown

Politecnico di Milano FEB 2019 – JUNE 2019
Teaching Assistant:
Master Course of *"Digital Systems and Design Methodologies 1"* held by Prof Fabrizio Ferrandi with 80 Students. Credits: 5 CFU. Course Evaluation: 2.7/4

Politecnico di Milano FEB 2019 – JUNE 2019
Project Tutor:
Bachelor Course of *"Prova Finale (Progetto di Reti Logiche) "* held by Prof Gianluca Palermo with 147 Students. Credits: 1 CFU. Course Evaluation: n.a.

Politecnico di Milano MAY 2022 – MAY 2022
Tutor:
"Hackathon: Informatica e Elementi di Informatica Medica" of the Bachelor course held by Prof Marco D. Santambrogio.

Politecnico di Milano OCT 2019 – NOV 2019
Tutor:
"Hackathon: Hack the NECSTCamp" held by Prof Marco D. Santambrogio.

FUNDED PROJECTS ACTIVITIES

GUIDO HORIZON ERC PoC Grants , Grant ID: 101112725 JANUARY 2024 – DECEMBER 2024
Work Package Leader:
WP Leader of the WP3 Simulation Execution of the HORIZON ERC PoC Grants *"GUIDO: Guidance Unified Interface for Deep-Space Spacecraft Operations"* by the European Research Council (ERC) Proof of Concept Grants. Politecnico di Milano funding amount: ~150K€.

National Centre for HPC, Big Data and Quantum Computing MARCH 2024 – ONGOING
Participant:
Part of the CENTRO NAZIONALE: National Centre for HPC, Big Data and Quantum Computing (HPC) in the context of the SPOKE 1 FUTURE HPC & BIG DATA as Assistant Professor for the program co-designing methodologies of hardware/softeare accelerators for heterogeneous and high-performance systems.

EVEREST EU H2020 PROJECT, CONTRACT NO. 957269 JANUARY 2023 – MARCH 2024

Task Leader:
Task Leader of the T3.1 Data allocation and storage in the WP3 Data management techniques of the European Project *"EVEREST: dEsign enVironmEnt foR Extreme-Scale big data analyTics on heterogeneous platforms"* by the Horizon 2020 EU Research & Innovation programme. Total budget ~5M€, Politecnico di Milano funding amount: ~650K€.

Huawei Technologies, Zurich Research Center FEB 2022 – JAN 2023
Participant, Post-Doc Researcher :
PostDoc researcher for the project entitled *"Templated Spatial Architectures"* by Huawei.

NVIDIA SEP 2021 – SEP 2022
Participant, Post-Doc Researcher :
PostDoc researcher on a grant entitled *"Software-programmable Domain Specific Architectures for Regular Expressions"* consisting on hardware donations from NVIDIA.

Tecnosens SEP 2019 – SEP 2020
Automation Infrastructure Lead and Hardware Developer :
Researcher for the project *"Software-defined hardware pipeline enabling high performance OCR over heterogeneous image streams"* from Tecnosens.

JULIGHT S.r.l. DEC 2018 – DEC 2019
Support:
Support researcher for the project *"Individuazione angolo vivo/morto"* from JULIGHT

IN2IT MAR 2018 – JULY 2018
Contributor to WP5:
Participant and contributor to the IN2IT: "*Internationalization by Innovative Technology European Project*", with a special focus on WP5, where, in particular, I have successfully completed the summary meeting "Development and exploitation of academy-industry/community cooperation" held in Kingston, (UK).

OTHER EXPERIENCE

NECSTLab - Politecnico di Milano CURRENT FROM JAN 2020
AMD-Xilinx License and Toolchain manager:
Responsible for managing, distributing, and handling AMD-Xilinx toolchains and licenses across machines and users.

NECSTLab - Politecnico di Milano CURRENT FROM JAN 2020
Coursera Sessions for FPGA-based courses:
Responsible for managing coursera private sessions linked to FPGA-based courses.

SCIENTIFIC PRODUCTIVITY AND IMPACT

Scientific Productivity: **40** publications (**31** entries on Scopus, **43** co-authors according to Scopus):

- Author/Co-author of **12** journal papers, of which **9** top-ranked **Q1** journal papers based on SCIMAGO (including ACM Transactions on Reconfigurable Technology and Systems, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Emerging Topics in Computing, ACM Computing Surveys, IEEE Journal of Biomedical and Health Informatics, Journal of Parallel and Distributed Computing);
- Author/Co-author of **27** scientific publications on peer-reviewed conferences among DAC, CGO, ICCD, FPGA;
- Author/Co-author of **1** Book Chapter.

Publication Impact:

Based on Google Scholar:	h-index **10**	citations **287**
Based on Scopus:	h-index **8**	citations **175**

Data collected on the 3rd January 2025, for Journals: Scimago; Conferences: CORE, GGS, and Conference Ranks.
Research Profiles:

- Dblp: https://dblp.org/pid/224/1533.html
- Scholar: https://scholar.google.it/citations?user=Y0VnEtkAAAAJ
- Orcid: https://orcid.org/0000-0002-5834-0812
- Scopus: https://www.scopus.com/authid/detail.uri?authorId=57203552342

Journal Publications

[J1] Marco Venere, Beatrice Branchini, **Davide Conficconi**, Donatella Sciuto, and Marco D. Santambrogio. "Rock the QASBA: Quantum Error Correction Acceleration via the Sparse Blossom Algorithm on FPGAs". In: *ACM Transactions on Reconfigurable Technology and Systems (TRETS)* 1.1 (2025). *Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking 2024*: **Q1**, SJR 0.8 [Scimago]., pp. 1–32. DOI: Accepted--To--Appear. URL: Accepted--To--Appear.

[J2] Francesco Peverelli, Daniele Paletti, and **Davide Conficconi**. "DFlows: A Flow-based Programming Approach for a Polyglot Design-Space Exploration Framework". In: *ACM Transactions on Reconfigurable Technology and Systems (TRETS)* 1.1 (2025). *Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking 2024*: **Q1**, SJR 0.8 [Scimago]., pp. 1–32. DOI: 10.1145/3717837. URL: https://doi.org/10.1145/3717837.

[J3] Alberto Zeni, Emanuele Del Sozzo, Eleonora D'Arnese, **Davide Conficconi**, and Marco D Santambrogio. "Starlight: A Kernel Optimizer for GPU Processing". In: *Journal of Parallel and Distributed Computing* (2023). *Citations*: 1 [Google Scholar], 1 [Scopus]. *Ranking 2023*: **Q1**, SJR 1.19 [Scimago]. DOI: 10.1016/j.jpdc.2023.104832. URL: https://doi.org/10.1016/j.jpdc.2023.104832.

[J4] Emanuele Del Sozzo, **Davide Conficconi**, and Kentaro Sano. "Across Time and Space: Senju's Approach for Scaling Iterative Stencil Loop Accelerators on Single and Multiple FPGAs". In: *ACM Transactions on Reconfigurable Technology and Systems (TRETS)* (2023). *Citations*: 3 [Google Scholar], 2 [Scopus]. *Ranking 2023*: **Q1**, SJR 0.802 [Scimago]. DOI: 10.1145/3634920. URL: https://doi.org/10.1145/3634920.

[J5] Giuseppe Sorrentino, Marco Venere, **Davide Conficconi**, Eleonora D'Arnese, and Marco D Santambrogio. "HEPHAESTUS: Codesigning and Automating 3D Image Registration on Reconfigurable Architectures". In: *ACM Transactions on Embedded Computing Systems (TECS)* 22.5s (2023). *Citations*: 5 [Google Scholar], 4 [Scopus]. *Ranking 2022*: **Q2**, SJR 0.8 [Scimago]. ISSN: 1539-9087. DOI: 10.1145/3607928. URL: https://doi.org/10.1145/3607928.

[J6] Raffaele Berzoini, Eleonora D'Arnese, **Davide Conficconi**, and Marco D. Santambrogio. "NERONE: the Fast Way to Efficiently Execute Your Deep Learning Algorithm at the Edge". In: *IEEE Journal of Biomedical and Health Informatics (J-BHI)* (2023). *Citations*: 3 [Google Scholar], 3 [Scopus]. *Ranking 2023*: **Q1**, SJR 1.964 [Scimago]., pp. 1252–1260. DOI: 10.1109/JBHI.2023.3296142. URL: https://doi.org/10.1109/JBHI.2023.3296142.

[J7] Eleonora D'Arnese, **Davide Conficconi**, Emanuele Del Sozzo, Luigi Fusco, Donatella Sciuto, and Marco D Santambrogio. "Faber: a Hardware/Soft-ware Toolchain for Image Registration". In: *IEEE Transactions on Parallel and Distributed Systems* (2022). *Citations*: 10 [Google Scholar], 9 [Scopus]. *Ranking 2022*: **Q1**, SJR 1.353 [Scimago]. DOI: 10.1109/TPDS.2022.3218898. URL: https://doi.org/10.1109/TPDS.2022.3218898.

[J8] Emanuele Del Sozzo, **Davide Conficconi**, Alberto Zeni, Mirko Salaris, Donatella Sciuto, and Marco Domenico Santambrogio. "Pushing the Level of Abstraction of Digital System Design: a Survey on How to Program FPGAs". In: *ACM Computing Surveys (CSUR)* (2022). *Citations*: 38 [Google Scholar], 23 [Scopus]. *Ranking 2022*: **Q1**, SJR 4.46 [Scimago]. DOI: 10.1145/3532989. URL: https://doi.org/10.1145/3532989.

[J9] **Davide Conficconi**, Emanuele Del Sozzo, Filippo Carloni, Alessandro Comodi, Alberto Scolari, and Marco Domenico Santambrogio. "An Energy-Efficient Domain-Specific Architecture for Regular Expressions". In: *IEEE Transactions on Emerging Topics in Computing* (2022). *Citations*: 17 [Google Scholar], 8 [Scopus]. *Ranking 2022*: **Q1**, SJR 1.353 [Scimago]. DOI: 10.1109/TETC.2022.3157948. URL: https://doi.org/10.1109/TETC.2022.3157948.

[J10] Daniele Parravicini, **Davide Conficconi**, Emanuele Del Sozzo, Christian Pilato, and Marco D Santambrogio. "CICERO: A Domain-Specific Architecture for Efficient Regular Expression Matching". In: *ACM Transactions on Embedded Computing Systems (TECS)* 20.5s (2021). *Citations*: 19 [Google Scholar], 14 [Scopus]. *Ranking 2021*: **Q2**, SJR 0.75 [Scimago]., pp. 1–24. DOI: 10.1145/3476982. URL: https://doi.org/10.1145/3476982.

[J11] Enrico Reggiani, Emanuele Del Sozzo, **Davide Conficconi**, Giuseppe Natale, Carlo Moroni, and Marco D Santambrogio. "Enhancing the scalability of multi-fpga stencil computations via highly optimized hdl components". In: *ACM Transactions on Reconfigurable Technology and Systems (TRETS)* 14.3 (2021). *Citations*: 17 [Google Scholar], 14 [Scopus]. *Ranking 2021*: **Q1**, SJR 0.88 [Scimago]., pp. 1–33. DOI: 10.1145/3461478. URL: https://doi.org/10.1145/3461478.

[J12] Yaman Umuroglu, **Davide Conficconi**, Lahiru Rasnayake, Thomas B Preusser, and Magnus Själander. "Optimizing bit-serial matrix multiplication for reconfigurable computing". In: *ACM Transactions on Reconfigurable Technology and Systems (TRETS)* 12.3 (2019). *Citations*: 27 [Google Scholar], 13 [Scopus]. *Ranking 2019*: **Q3**, SJR 0.26 [Scimago]., pp. 1–24. DOI: 10.1145/3337929. URL: https://doi.org/10.1145/3337929.

Conference Publications

[C1] Giuseppe Sorrentino, Paolo S. Galfano, Eleonora D'Arnese, and **Davide Conficconi**. "VOTED – Versal Optimization Toolkit for Education and Heterogeneous Systems Development". In: *2025 IEEE International Symposium on Circuits and Systems (ISCAS). Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking*: GGS Class: 2, Rating: A-, LiveSHINE: A+, MA: A- [GSS]. 2025, pp. 1–5. DOI: Accepted--To--Appear.

[C2] Andrea Somaini, Filippo Carloni, Giovanni Agosta, Marco D Santambrogio, and **Davide Conficconi**. "Combining MLIR Dialects with Domain-Specific Architecture for Efficient Regular Expression Matching". In: *IEEE/ACM International Symposium on Code Generation and Optimization. Acceptance Rate*: XX% (XX/XXX), *Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking*: A [CORE], GGS: 2, CORE:A, LiveSHINE:A+, MA:A- [GSS]. 2025. DOI: 10.1145/3696443.3708916.

[C3] Francesco Peverelli, Alessandro Verosimile, **Davide Conficconi**, Andrea Damiani, and Marco Santambrogio. "SATL: A Spatial Architecture Rapid Prototyping Framework for Irregular Applications Acceleration". In: *IEEE International Conference on Computer Design. Acceptance Rate*: 36.82% (102/277), *Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking*: A2 [Qualis], GGS: 2, LiveSHINE:A-, MA:A- [GSS]. 2024. DOI: 10.1109/ICCD63220.2024.00074. URL: https://doi.org/10.1109/ICCD63220.2024.00074.

[C4] Paolo S. Galfano, Giuseppe Sorrentino, Eleonora D'Arnese, and **Davide Conficconi**. "Co-Designing a 3D Transformation Accelerator for Versal-Based Image Registration". In: *IEEE International Conference on Computer Design. Acceptance Rate*: 36.82% (102/277), *Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking*: A2 [Qualis], GGS: 2, LiveSHINE:A-, MA:A- [GSS]. 2024. DOI: 10.1109/ICCD63220.2024.00041. URL: https://doi.org/10.1109/ICCD63220.2024.00041.

[C5] Filippo Carloni, **Davide Conficconi**, and Marco D Santambrogio. "ALVEARE: a Domain-Specific Framework for Regular Expressions". In: *61st ACM/IEEE Design Automation Conference (DAC '24). Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking*: A [CORE], GGS: 2, CORE:A, LiveSHINE:A++, MA:A++ [GSS]. 2024, pp. 193–206. DOI: 10.1145/3649329.3657378. URL: https://doi.org/10.1145/3649329.3657378.

[C6] Niccolò Nicolosi, Francesco Renato Negri, Francesco Pesce, Francesco Peverelli, **Davide Conficconi**, and Marco Domenico Santambrogio. "PSyGS Gen A Generator of Domain-Specific Architectures to Accelerate Sparse Linear System Resolution". In: *2024 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW). Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking*: MA: C [GSS], Qualis: B3 [Conference Ranks]. IEEE. 2024, pp. 41–47. DOI: 10.1109/IPDPSW63119.2024.00015. URL: https://doi.org/10.1109/IPDPSW63119.2024.00015.

[C7] Federico Valentino, Beatrice Branchini, **Davide Conficconi**, Donatella Sciuto, and Marco D. Santambrogio. "An Accurate Union Find Decoder for Quantum Error Correction on the Toric Code". In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW). Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking*: MA: C [GSS], Qualis: B3 [Conference Ranks]. 2024, pp. 99–105. DOI: 10.1109/IPDPSW63119.2024.00032. URL: https://doi.org/10.1109/IPDPSW63119.2024.00032.

[C8] Marco Venere, Valentino Guerrini, Beatrice Branchini, **Davide Conficconi**, Donatella Sciuto, and Marco D. Santambrogio. "Towards the Acceleration of the Sparse Blossom Algorithm for Quantum Error Correction". In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW). Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking*: MA: C [GSS], Qualis: B3 [Conference Ranks]. 2024, pp. 106–110. DOI: 10.1109/IPDPSW63119.2024.00033. URL: https://doi.org/10.1109/IPDPSW63119.2024.00033.

[C9] Roberto Alessandro Bertolini, Filippo Carloni, **Davide Conficconi**, and Marco D. Santambrogio. "POCA: a PYNQ Offloaded Cryptographic Accelerator on Embedded FPGA-based Systems". In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW). Citations*: 0 [Google Scholar], 0 [Scopus]. *Ranking*: MA: C [GSS], Qualis: B3 [Conference Ranks]. 2024, p. 194. DOI: 10.1109/IPDPSW63119.2024.00054. URL: https://doi.org/10.1109/IPDPSW63119.2024.00054.

[C10] Luisa Cicolini, Filippo Carloni, Marco D Santambrogio, and **Davide Conficconi**. "One Automaton To Rule Them All: Beyond Multiple Regular Expressions Execution". In: *IEEE/ACM International Symposium on Code Generation and Optimization. Acceptance Rate*: 32.4% (37/114), *Citations*: 1 [Google Scholar], 1 [Scopus]. *Ranking*: A [CORE], GGS: 2, CORE:A, LiveSHINE:A+, MA:A- [GSS]. 2024, pp. 193–206. DOI: https://doi.org/10.1109/CGO57630.2024.10444810.

[C11] Giuseppe Sorrentino, Marco Venere, Eleonora D'Arnese, **Davide Conficconi**, Isabella Poles, and Marco D Santambrogio. "ATHENA: a GPU-based Framework for Biomedical 3D Rigid Image Registration". In: *IEEE Biomedical Circuits and Systems Conference (BioCAS). Citations*: 1 [Google Scholar], 1 [Scopus]. *Ranking*: MA: C [GSS]. 2023, pp. 1–5. DOI: https://doi.org/10.1109/BioCAS58349.2023.10388589.

[C12] Beatrice Branchini, **Davide Conficconi**, Donatella Sciuto, and Marco Santambrogio. "The Hitchhiker's Guide to FPGA-Accelerated Quantum Error Correction". In: *2023 IEEE International Conference on Quantum Computing and Engineering (QCE)*. Vol. 02. *Citations*: 4 [Google Scholar], 3 [Scopus]. *Ranking*: Qualis: B3 [Conference Ranks]. 2023, pp. 338–339. DOI: 10.1109/QCE57702.2023.10271. URL: https://doi.org/10.1109/QCE57702.2023.10271.

[C13] Marco Venere, Giuseppe Sorrentino, Beatrice Branchini, **Davide Conficconi**, Elisabetta Di Nitto, Donatella Sciuto, and Marco Santambrogio. "On the Design and Characterization of Set Packing Problem on Quantum Annealers". In: *IEEE EUROCON 2023 International Conference on Smart Technologies. Citations*: 3 [Google Scholar], 2 [Scopus]. *Ranking*: Qualis: B3 [Conference Ranks]. 2023, pp. 695–700. DOI: 10.1109/EUROCON56442.2023.10199096. URL: https://doi.org/10.1109/EUROCON56442.2023.10199096.

[C14] Beatrice Branchini, **Davide Conficconi**, Francesco Peverelli, Donatella Sciuto, and Marco Santambrogio. "A Bird's Eye View on Quantum Computing: Current and Future Trends". In: *IEEE EUROCON 2023 International Conference on Smart Technologies. Citations*: 3 [Google Scholar], 3 [Scopus]. *Ranking*: Qualis: B3 [Conference Ranks]. 2023, pp. 689–694. DOI: 10.1109/EUROCON56442.2023.10198957. URL: https://doi.org/10.1109/EUROCON56442.2023.10198957.

[C15] Roberto Alessandro Bertolini, Filippo Carloni, and **Davide Conficconi**. "Co-designing an FPGA-Accelerated Encryption Library With PYNQ: The Pynqrypt Case Study". In: *IEEE EUROCON 2023 International Conference on Smart Technologies. Citations*: 1 [Google Scholar], 1 [Scopus]. *Ranking*: Qualis: B3 [Conference Ranks]. 2023, pp. 683–688. DOI: 10.1109/EUROCON56442.2023.10198938. URL: https://doi.org/10.1109/EUROCON56442.2023.10198938.

[C16] Filippo Carloni, Leonardo Panseri, **Davide Conficconi**, Mattia Sironi, and Marco D. Santambrogio. "Enabling Efficient Regular Expression Matching at the Edge through Domain-Specific Architectures". In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW). Citations*: 1 [Google Scholar], 1 [Scopus]. *Ranking*: MA: C [GSS], Qualis: B3 [Conference Ranks]. 2023, pp. 71–74. DOI: 10.1109/IPDPSW59300.2023.00023. URL: https://doi.org/10.1109/IPDPSW59300.2023.00023.

[C17] Filippo Carloni, **Davide Conficconi**, Ilaria Moschetto, and Marco D. Santambrogio. "YARB: A Methodology to Characterize Regular Expression Matching on Heterogeneous Systems". In: *2023 IEEE International Symposium on Circuits and Systems (ISCAS). Citations*: 2 [Google Scholar], 2 [Scopus]. *Ranking*: GGS Class: 2, Rating: A-, LiveSHINE: A+, MA: A- [GSS]. 2023, pp. 1–5. DOI: 10.1109/ISCAS46773.2023.10181547. URL: https://doi.org/10.1109/ISCAS46773.2023.10181547.

[C18] Emanuele Del Sozzo, **Davide Conficconi**, Marco D. Santambrogio, and Kentaro Sano. "Senju: A Framework for the Design of Highly Parallel FPGA-based Iterative Stencil Loop Accelerators". In: *Proceedings of the 2023 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays. Citations*: 4 [Google Scholar], 0 [Scopus]. *Ranking*: Class 2, Rating A, LiveSHINE: A, MA: A [GSS]. 2023, p. 233. DOI: 10.1145/3543622.3573170. URL: https://doi.org/10.1145/3543622.3573170.

[C19] Francesco Peverelli, **Davide Conficconi**, Davide Basilio Bartolini, Alberto Scolari, and Marco D. Santambrogio. "Characterizing Molecular Dynamics Simulation on Commodity Platforms". In: *2022 IEEE International Symposium on Workload Characterization (IISWC). Acceptance Rate*: 47.9% (23/48). *Citations*: 3 [Google Scholar], 3 [Scopus]. *Ranking*: Rating A-, MA: A- [GSS]. 2022, pp. 65–78. DOI: 10.1109/IISWC55918.2022.00016. URL: https://doi.org/10.1109/IISWC55918.2022.00016.

[C20] Raffaele Berzoini, Eleonora D'Arnese, and **Davide Conficconi**. "On How to Push Efficient Medical Semantic Segmentation to the Edge: the SENECA approach". In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW). Citations*: 3 [Google Scholar], 2 [Scopus]. *Ranking*: MA: C [GSS], Qualis: B3 [Conference Ranks]. 2022. DOI: 10.1109/IPDPSW55747.2022.00027. URL: https://doi.org/10.1109/IPDPSW55747.2022.00027.

[C21] Daniele Paletti, Francesco Peverelli, and **Davide Conficconi**. "Online Learning RTL Synthesis for Automated Design Space Exploration". In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW). Citations*: 3 [Google Scholar], 3 [Scopus]. *Ranking*: MA: C [GSS], Qualis: B3 [Conference Ranks]. 2022. DOI: 10.1109/IPDPSW55747.2022.00021. URL: https://doi.org/10.1109/IPDPSW55747.2022.00021.

[C22] Eleonora D'Arnese, Emanuele Del Sozzo, **Davide Conficconi**, and Marco D Santambrogio. "Exploiting Heterogeneous Architectures for Rigid Image Registration". In: *IEEE Biomedical Circuits and Systems Conference (BioCAS). Citations*: 6 [Google Scholar], 4 [Scopus]. *Ranking*: MA: C [GSS]. 2021, pp. 1–5. DOI: 10.1109/BioCAS49922.2021.9645026. URL: https://doi.org/10.1109/BioCAS49922.2021.9645026.

[C23] Giulia Gerometta, **Davide Conficconi**, and Marco Domenico Santambrogio. "On How FPGAs are Changing the Computer Security Panorama: An Educational Survey". In: *IEEE 6th International Forum on Research and Technology for Society and Industry (RTSI). Citations*: 2 [Google Scholar], 1 [Scopus]. *Ranking*: n.a. . 2021, pp. 80–85. DOI: 10.1109/RTSI50628.2021.9597337. URL: https://doi.org/10.1109/RTSI50628.2021.9597337.

[C24] Daniele Paletti, **Davide Conficconi**, and Marco D Santambrogio. "Dovado: An Open-Source Design Space Exploration Framework". In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW). Citations*: 8 [Google Scholar], 5 [Scopus]. *Ranking*: MA: C [GSS], Qualis: B3 [Conference Ranks]. 2021, pp. 128–135. DOI: 10.1109/IPDPSW52791.2021.000271. URL: https://doi.org/10.1109/IPDPSW52791.2021.00027.

[C25] **Davide Conficconi**, Eleonora D'Arnese, Emanuele Del Sozzo, Donatella Sciuto, and Marco D Santambrogio. "A Framework for Customizable FPGA-based Image Registration Accelerators". In: *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays. Acceptance Rate*: 23.2% (26/111). *Citations*: 20 [Google Scholar], 17 [Scopus]. *Ranking*: GGS Class 2, Rating A, LiveSHINE: A, MA: A [GSS]. 2021, pp. 251–261. DOI: 10.1145/3431920.3439291. URL: https://doi.org/10.1145/3431920.3439291.

[C26] Lorenzo Di Tucci, **Davide Conficconi**, Alessandro Comodi, Steven Hofmeyr, David Donofrio, and Marco D Santambrogio. "A parallel, energy efficient hardware architecture for the merAligner on FPGA using Chisel HCL". In: *IEEE International*

Parallel and Distributed Processing Symposium Workshops (IPDPSW). *Citations*: 12 [Google Scholar], 9 [Scopus]. *Ranking*: MA: C [GSS], Qualis: B3 [Conference Ranks]. 2018, pp. 214–217. DOI: 10.1109/IPDPSW.2018.00041. URL: https://doi.org/10.1109/IPDPSW.2018.00041.

[C27] Alessandro Comodi, **Davide Conficconi**, Alberto Scolari, and Marco D Santambrogio. "TiReX: Tiled regular expression matching architecture". In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. *Citations*: 17 [Google Scholar], 13 [Scopus]. *Ranking*: MA: C [GSS], Qualis: B3 [Conference Ranks]. 2018, pp. 131–137. DOI: 10.1109/IPDPSW.2018.00028. URL: https://doi.org/10.1109/IPDPSW.2018.00028.

Book Chapters

[B1] Eleonora D'Arnese, **Davide Conficconi**, Marco Domenico Santambrogio, and Donatella Sciuto. "Reconfigurable architectures: the shift from general systems to domain specific solutions". In: *Emerging Computing: From Devices to Systems. Looking Beyond Moore and Von Neumann*. Ed. by Anupam Chattopadhyay Mohamed M. Sabry Aly. *Citations*: 19 [Google Scholar], 0 [Scopus]. *Ranking* : n.a. . Singapore: Springer Nature Singapore, 2023, pp. 435–456. ISBN: 978-981-16-7487-7. DOI: 10.1007/978-981-16-7487-7_14. URL: https://doi.org/10.1007/978-981-16-7487-7_14.

AWARDS AND RECONGNITION

2025 **European Talent Academy fellowship**, selected among the best 7 researchers from Politecnico di Milano to join the program. Theme: "*Water and Food for Healthy and Resilient Societies*". This fellowship is a training programme among Politecnico di Milano, Imperial College of London and Technische Universität München to support top researchers for joint project proposals

2025 **ACM Artifacts** of *Open Research Objects*, *Research Objects Reviewed*, *Results Reproduced* for [C2].

2024 **Supervisor of a Winner Team of AMD Open Hardware Design Contest**
From FPGA To AI Engine: Beyond Mutual Information Limits, G. Brunetta, F. Santambrogio

2024 **Best Poster** award at RAW 2024 for [C8].

2024 **IEEE Artifacts** of *Open Research Objects*, *Research Objects Reviewed*, *Results Reproduced* for [C7].

2024 **Interdisciplinary Ph.D. Scholarship funds** for a *joint program* among *Space Systems-Information Systems* departments of Politecnico di Milano.

2024 **ACM Artifacts** *of Available, Reusable, Validated & Reproduced* for [C10]

2023 **Co-Supervisor of a Winner Team of AMD Open Hardware Design Contest**
Heterogeneous Highly Integrated Systems for Image Registration, G. Sorrentino, P. Galfano

2023 **HiPEAC Summer School ACACES Grant**

2023 **IEEE Artifacts** of *Open Research Objects*, *Research Objects Reviewed*, *Results Reproduced* for [C16]

2023 **Young People Programme** award at DATE'23

2022 **IEEE Artifacts** of *Open Research Objects*, i.e., research artifact open-source, for [C19]

2022 **Co-Supervisor of a Winner Team of Xilinx Open Hardware Design Contest**
A Journey to the center of the 3D Space, G. Sorrentino, M. Venere

2022 **IBM Best PhD Intern Presentation** at Cloud & AI Systems Research (CAISR) department Intern Symposium July '22

2022 **First Place IEEE 2022 Lance Stafford Larson Award** on [C25]

2022 **ASPLOS 2022 Student Travel Award**

2021 **NVIDIA Academic Hardware Grant Program** *"Software-programmable Domain Specific Architectures for Regular Expressions"*

2021 **ACM Artifacts** *of Available, Reusable, Reproduced* for [C25]

2019 **Finalist of Xilinx Open Hardware Design Contest**
IRON Image RegistratiOn oN FPGA

2018 **First Prize Shark Tank** Internal Interns Competition at Xilinx Dublin with "*Deep Breath: Measuring Precisly the Air Pollution*"

2017 **Finalist of Xilinx Open Hardware Design Contest**
TiReX: Tiled Regular eXpression matching architecture

2017 **Scholarship for High Merits at PoliMi**
2018 Partial tuition waiver for high academic performance

2017 **Category Winners Xilinx PYNQ Hackathon at PoliMi**
Smart glove for remote controlling

CONFERENCE ACTIVITIES

Committee and Organization

PROGRAM CHAIR	RAW '25
PROGRAM COMMITTEE	FCCM '25, FPL '25,HEART '25, SAC'25 - EMBS Track,RAW '25,EUROCON '25 HPCC '24, PACRIM '24 FPL '24, FCCM '24, GLSVLSI '24, HEART '24, SAC'24 - EMBS Track , RAW '24 ISPA '23, GLSVLSI '23, RAW '23 RAW '22
ARTIFACT EVALUATION CHAIR	RAW '24 RAW '23
ARTIFACT EVALUATION COMMITTEE	ASPLOS '25, CGO '25 CGO '24 MICRO '23, ASPLOS '23, CGO '23, PLDI '23 ASPLOS '22
PHD FORUM COMMITTEE	DATE '25
POSTER COMMITTEE	IISWC '24
SESSION CHAIR	"Quantum Computing and Backends" at CGO '25 "Accelerators" at IPDPS '24 "Architecture and Toolflow" at at RAW '24, "Computer science, quantum solutions and digital twins" at EUROCON '23 RAW '23, RAW '21
TUTORIAL ORGANIZER	"Faber: a Hardware/Software Toolchain for Image Registration" at EUROCON '23
BOOTCAMP ORGANIZER	Chisel Bootcamp at ASAP '18
VOLUNTEER	DATE '21, DATE '19

External Reviewer

REVIEWER	ISCAS '25 ISCAS '24, FPL '23, AFRICON '23 EUROCON '23 ISPA '22,HEART '22, 2xDATE'22, DAC '22 DATE '21, FCCM '20, 2xICS '20
SUBREVIEWER	2xDAC '21, RAID '21, 2xDAC '20, DATE '20, RAW '20, FPL '20, CODES+ISSS '19, ReConFig '19

Attendance

2025 HPCA'25, CGO'25
2024 DAC'24, IPDPS'24, RAW'24, HPCA'24, CGO'24, CC'24, IWCM^{2}Workshop'24
2023 DATE'23, RAW'23
2022 ASPLOS '22, NOPE'22, DATE'22, GTC '22, HEART'22, IPDPS'22, FPT'22
2021 H^{2}RC '21, ESWEEK '21, GTC '21, Xilinx Adapt'21, DATE'21, FPGA'21, RAW'21, ISCA'21, ISVLSI'21
2020 HOTI '20, FPL'20, DAC'20, Xilinx Adapt'20
2019 DATE'19, ICS'19, PhD Workshop on "Next-Generation Cloud Infrastructure" MSR Cambridge
2018 RAW'18
2017 RAW'17

JOURNAL ACTIVITIES

APRIL 2023 - DECEMBER 2024

Guest Editor:

Guest Editor for the Special Issue on Secure and Efficient Distributed Computation for Emerging Systems on the Edge (SUNRISE) on Elsevier Journal of Parallel and Distributed Computing (JPDC).

SEPT. 2020 - CURRENT

Reviewer:

Revising 40+ manuscripts across different journals:
ACM Transactions on Reconfigurable Technology and Systems (TRETS): 2025, 2024, 2023;
IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD): 2025, 2024, 2022;
Elsevier Computer Networks (COMNET): 2024
ACM Transactions on Architecture and Code Optimization (TACO): 2024;
IEEE Transaction on Parallel and Distributed Sytems (TPDS): 2024, 2021, 2020;
IEEE Transactions on Very Large Scale Integration (VLSI) Systems: 2024, 2023;
IEEE Transactions on Emerging Topics in Computing (TETC): 2024, 2023;
IEEE Access: 2024, 2022, 2021;
IEEE Embedded Systems Letters (ESL): 2024, 2023;
Elsevier SoftwareX: 2024;
ACM Transactions on Embedded Computing Systems (TECS): 2023, 2022;
IEEE IT Professional (ITPro): 2023;
Elsevier Computes and Security (COSE):2021;
Elsevier Microprocessors and Microsystems (MICPRO):2021 ;

ACM Transactions on Design Automation of Electronic Systems (TODAES): 2021;

EXTERNAL EXPERT ACTIVITIES

PHD REFEREE	Thesis "Graph-based techniques and strategies for diagnosis and characterization of neurodegenerative diseases ", 2023, by Laura Hernández Lorenzo, Universidad Complutense de Madrid, Advisors: J. Ayala, J. Antem.
PROPOSAL REVIEW	Swiss National Science Foundation (SNSF) 2023
AWARD REVIEWERS	IEEE CS Larson Award reviewer for 2023 fall cycle

COMMUNICATION SKILLS

TALK

2024	"From FPGA To AI Engine: Beyond Mutual Information Limits", at AMD Open Hardware Competition '24
2023	"From Domain-Specific to Quantum Computing: the Role of Reconfigurable Systems", at IEEE EUROCON 2023,
2023	"Enabling Efficient Regular Expression Matching at the Edge through Domain-Specific Architectures", at RAW '23
2022	"Characterizing the CloudFPGA System", at CAISR Interns Syposium, IBM Research, Zurich (CH)
2021	"On the Role of Reconfigurable Systems in Domain Specific Computing", Colloquia Doctoralia at PoliMi, Milan (ITA).
2021	"A Framework for Customizable FPGA-based Image Registration Accelerators", at H²RC '21
2021	"Dovado: An Open-Source Design Space Exploration Framework", at RAW '21
2021	"A Framework for Customizable FPGA-based Image Registration Accelerators", at FPGA '21
2018	"Deep Breath", Shark Tank at Xilinx, Dublin (IE).
2018	"TiReX: Tiled Regular eXpression matching architecture", at RAW '18

INVITED TALK

2024	"Accelerating Iterative Rigid Medical Image Registration via Domain-Specialization: from Embedded to High-Performance Systems", at AMD-Xilinx, June 2024, San Jose, California (US) "Exploring Domain-Specialization in the Regular Expression Field End ", at AMD-Xilinx June 2024, San Jose, California (US) "Domain-Specific Computing Research Line at NECSTLab", Feb'24, virtual/online held to international institutions.
2023	"Intro to the NECSTLab and the NECST Research Line Fair Event (NRLFE)", at several companies (e.g., Bosh, Edutech District, Bending Spoons, Amazon) in presence and online, NRLFE, Politecnico di Milano, Milan (IT) July 2023, Torino, (ITA)

2023 "Domain-Specific Computing Research Line at NECSTLab", at Boston University, Boston, MA (USA).
2023 "Faber: Hardware/Software Toolchain for Image Registration", at Northeastern University, Boston, MA (USA).

2022 "On the Role of Reconfigurable Systems in Domain Specific Computing", NECST Friday Talk at PoliMi, Milan (ITA).
2022 "Intro to the NECSTLab and the NECST Research Line Fair Event (NRLFE)", at several companies (e.g., Mindway, ABE Elettronica, Xlogic, Techedge) in presence and online, NRLFE, Politecnico di Milano, Milan (IT)
2022 "Domain-Specific Computing Research Line at NECSTLab", at Huawei Research at Polimi, Milan (ITA)
2022 "Faber: Hardware/Software Toolchain for Image Registration", at Northwestern University, IL (USA).
2022 "Domain-Specific Computing Research Line at NECSTLab", at Northwestern University, IL (USA).
2022 "Software-programmable Domain-Specific Architectures for Regular Expressions", virtually held to NVIDIA DPU team.
2022 "Faber: Hardware/Software Toolchain for Image Registration", at University of Illinois at Chicago, IL (USA).
2022 "Domain-Specific Computing Research Line at NECSTLab", at University of Illinois at Chicago, IL (USA).
2022 "Faber: Hardware/Software Toolchain for Image Registration", virtually held to international institutions: Microsoft Research, Lawrence Berkeley National Laboratory, Xilinx Inc.

2020 "DRACO: Domain-specific Reconfigurable Architecture Computer Organization", PoliMi, Milan (ITA).

2019 "DRACO: Domain-specific Reconfigurable Architecture Computer Organization", Open Networking Foundation (ONF), Menlo Park, CA (USA).
2019 "DRACO: Domain-specific Reconfigurable Architecture Computer Organization", Lawrence Berkeley National Laboratory, Berkeley, CA (USA).
2019 "DRACO: Domain-specific Reconfigurable Architecture Computer Organization", Xilinx, San Josè, CA (USA).
2019 "TiReX: Tiled Regular eXpression matching architecture", Xilinx, San Josè, CA (USA).
2019 "DRACO: Domain-specific Reconfigurable Architecture Computer Organization", Xilinx, San Josè, CA (USA).

2018 "TiReX: Tiled Regular eXpression matching architecture", Xilinx, San Josè, CA (USA).

2017 "TiReX: Tiled Regular eXpression matching architecture", Microsoft Research at PoliMi, Milan (ITA)
2017 "TiReX: Tiled Regular eXpression matching architecture", Xilinx, San Josè, CA (USA).

POSTER

2023 "Hardware/Software Acceleration of Heuristic-based Image Registration on Heterogeneous Systems", 19th International Summer School on Advanced Computer Arch. and Compilation for High-performance Embedded Systems '23, Fiuggi (ITA)
2023 "On the Role of Reconfigurable Systems in Domain Specific Computing", DATE'23 PhD Forum, Antwerp (BE)

2019 "DRACO: Domain specific Reconfigurable Architecture Computer Organization", PhD Workshop on Next-Generation Cloud Infrastructure '19, MSR, Cambridge

2018 "TiReX: Tiled Regular eXpression matching architecture", Xilinx, San Josè, CA (USA).

SEMINARS

2019 "On how to develop from software to hardware for the ZYNQ technology and the Ultra96", Tecnosens and Imavis at PoliMi, Milan (ITA).

LECTURES
Advanced Computer Architectures '24 till '20
CPS Creative Lab '23, '22
FPGA101 '24 spring, '23 fall, '23 spring, '22 fall
Hardware and Accelerators: FPGAs for AI '22
FPGAcademy '22 spring-'21-'20
Digital System and Design Methodologies 1 '19

COURSES
Participant "Pitching your research to key audiences" by H. Gustaffon, NTNU, 2020

Participant "Embracing Diversity" 1+2 by IN2IT Platform, 2018

Participant "English for Internationalization" 1+2 by IN2IT Platform, 2018

Participant "Startup 101" by S. Notargiacomo, PoliMi, 2017

WORKSHOP
Participant"The 5 Chairs of Leadership" and "Assertiveness", L. Evans, Milan, May'23
Participant "Active Learning and Feedback for soft skills", METID, Milan, Nov'19
Participant "Presentation skills and storyline building", BCG, Milan, Nov'19
Participant "PhD Workshop on Next-Gen. Cloud Infrastructure", MSR, Cambridge, Nov'19

Participant "Design Thinking", Bosch, Feb'19

LANGUAGES
Italian Native, English Fluent, German Beginner

COMMISSION OF TRUST

2024 Apil, **Ph.D thesis defense committee member**, "Graph-based techniques and strategies for diagnosis and characterization of neurodegenerative diseases", Laura HERNÁNDEZ LORENZO, UNIVERSIDAD COMPLUTENSE DE MADRID.

2023 Nov-Dec, **External referee Ph.D. thesis** in Computer Science and Engineering, Universidad Complutense de Madrid.

2024 April, **Master thesis defense committee member** in Computer Science and Engineering, 11 students, Politecnico di Milano.

2023 October, **Master thesis defense committee member** in Computer Science and Engineering, 10 students, Politecnico di Milano.

2023 May, **Master thesis defense committee member** in Computer Science and Engineering, 11 students, Politecnico di Milano.

ADVISING ACTIVITIES

PhD Advising Activities

ADVISOR Dec 2023 - Ongoing *G. Sorrentino*, Politecnico di Milano
"Towards Federated Learning for Versal-based Healthcare Procedures"
Co-Advisor: *M. D. Samtabrogio*

CO-ADVISOR Dec 2024 - Ongoing *O. Regantini*, Politecnico di Milano
"Power-Efficient Computing Units for On-Board Autonomous Guidance for Deep-Space Applications"
Advisor: *A. Morselli*

Master Thesis Advisor

2024 DECEMBER **"An Emulation-based Approach for Fast DSE of a Domain-Specific Architecture for RE Matching"**
Student: *T. Van Den Weghe*, Politecnico di Milano
Politecnico di Milano

2023 OCTOBER **"One Automaton To Rule Them All: Enabling Multiple Regular Expressions Execution"**
Student: *L. Cicolini*, Politecnico di Milano
Co-Advisor: *F. Carloni*

2023 JULY **"HEPHAESTUS: an FPGA-based Framework for 3D Image Registration'**
Student: *G. Sorrentino*, Politecnico di Milano
Co-Advisor: *E. D'Arnese*

2023 APRIL **"On the Feasibility of Optimizing ML-Based Intrusion Detection for CAN on Real-world Hardware Platforms"**
Student: *E. Massaro*, Politecnico di Milano
Co-Advisor: *S. Longari*

Master Thesis Co-Advisor

2024 DECEMBER **"Automata Minimization and Beyond: A Systematic Evaluation of DFA-based Pattern Matching"**
Student: *F. G. Del Nero*, University of Illinois at Chicago
Advisor: *M. D. Santambrogio*
Co-Advisor: *F. Carloni, L. Cicolini*

2022 OCTOBER **"AutoREX: a Methodology for Regular Expressions Benchmarking on Heterogeneous Architectures"**
Student: *I. Moschetto*, Politecnico di Milano
Advisor: *M. D. Santambrogio*
Co-Advisor: *F. Carloni*

2022 APRIL **"YBoost: a framework to accelerate YARA rules pattern matching using FPGAs"**
Student: *A. Furlan*, Politecnico di Milano
Advisor: *S. Zanero*
Co-Advisor: *M. Carminati, M. Polino*

2021 OCTOBER **"Alveare: A Novel Mixed HW-SW Framework for Efficient Execution of Regular Expressions"**
Student: *F. Carloni*, Politecnico di Milano
Advisor: *M. D. Santambrogio*

Completed Student (Grad. and Undergrad.) Research Projects

2024 **"Orbit Boost: Accelerating Satellite Autonomous Path Computation"**

Student: *M. Laurenzi, A. A. Marina*, Politecnico di Milano

2024 **"Towards AIE-based Mutual Information for Image Registration"**
Student: *G. Brunetta, F. Santambrogio*, Politecnico di Milano
Co-Supervisor: *G. Sorrentino*

2024 **"Towards an AI Engine-based library for similarity metrics computation"**
Student: *D. Ettori, F. Mansutti*, Politecnico di Milano
Co-Supervisor: *G. Sorrentino*

2024 **"Versal System Exploration: Benchmark Suite for AI Engine"**
Student: *E. Cabai*, Politecnico di Milano
Co-Supervisor: *G. Sorrentino*

2024 **"AXI4 High-Speed Communication for Microprocessors and RegEx Architecture"**
Student: *M. La Barbera, G. Lotto*, Politecnico di Milano
Co-Supervisor: *F. Carloni*

2024 **"Leveraging spatial architectures for the parallelization of the MFSA"**
Student: *P. Poggi*, Politecnico di Milano
Co-Supervisor: *F. Carloni*

2024 **"SmartNIC Exploration on AMD FPGAs"**
Student: *E. Carlotto*, Politecnico di Milano
Co-Supervisor: *F. Carloni*

2024 **"An Analysis of the State of the Art in High Peformance RISC-V Computing"**
Student: *R. A. Bertolini*, Politecnico di Milano

2024 **"Automata Minimization and Beyond"**
Student: *F. G. Del Nero*, Politecnico di Milano, University of Illinois at Chicago
Co-Supervisor: *F. Carloni, L. Cicolini*

2024 **"Exploiting Heterogeneous Highly Integrated Systems for Image Registration"**
2023 Student: *P. Galfano, G. Sorrentino*, Politecnico di Milano
Co-Supervisor: *E. D'Arnese*

2024 **"Hardware/Software Optimization for Regular Expressions Execution on Zynq Devices"**
2023 Student: *A. Somaini*, Politecnico di Milano
Co-Supervisor: *F. Carloni*

2023 **"Quantum Error Correction: an FPGA-based approach"**
Student: *M. Venere, V. Guerrini, P. Giannoccaro*, Politecnico di Milano
Co-Supervisor: *B. Branchini*

2023 **"Quantum Error Correction: an FPGA-based approach"**
Student: *F. Valentino, F. Scroccarello*, Politecnico di Milano
Co-Supervisor: *B. Branchini*

2023 **"Hardware/Software Optimization for Regular Expressions Execution on Zynq Devices"**
Student: *S. Mannarino, F. Vinco*, Politecnico di Milano
Co-Supervisor: *F. Carloni*

2023 **"A 3D Image Transformation Accelerator"**
Student: *C. Grasso*, Politecnico di Milano

2023 **"3D Image Registration via HBM FPGAs"**
Student: *E. Poggiolini*, Politecnico di Milano

2023 **"Symmetric Encription on Edge Zynq devices"**
2022 Student: *R. A. Bertolini*, Politecnico di Milano

2023 **"On the Characterization of Automata Minimization effects on CPUs' execution times and memory effects."**
Student: *F. G. Del Nero, A. Infantino*, Politecnico di Milano
Co-Supervisor: *F. Carloni*

2023 **"3D Image Registration"**
2022 Student: *G. Sorrentino, M. Venere*, Politecnico di Milano
Co-Supervisor: *E. D'Arnese*

2023 **"Domain-Specific Compiler Optimizations for REs"**
2022 Student: *L. Cicolini*, Politecnico di Milano
Co-Supervisor: *F. Carloni*

2022 **"Chipyard on VC707"**
Student: *O. S. Aragon Celis, J. Di Salvo, M. Carrara*, Politecnico di Milano
Co-Supervisor: *F. Peverelli*

2022 **"PYNQ API Generator"**
Student: *M. Ferrè, S. Iachini*, Politecnico di Milano

2022 **"Accelerating CNN Inference at the Edge "**
2021 Student: *R. Berzoini*, Politecnico di Milano
Co-Supervisor: *E. D'Arnese*

2021 **"Approximating DSE with Online Learning "**
Student: *D. Paletti*, Politecnico di Milano
Co-Supervisor: *F. Peverelli*

2021 **"Bluespec RISC-V on FPGAs"**
Student: *R. Nannini*, Politecnico di Milano
Co-Supervisor: *E. Del Sozzo*

2021 **"Compiler-based range analysis"**
Student: *C. Sguanci*, Politecnico di Milano
Co-Supervisor: *E. Del Sozzo*

2021 **"GEM: Gradient Enabled Mutual information "**
2020 Student: *L. Fusco*, Politecnico di Milano
Co-Supervisor: *E. D'Arnese, E. Del Sozzo*

2020 **"How FPGAs are changing the Computer Security Panorama"**
Student: *G. Gerometta*, Politecnico di Milano

2020 **"DSE framework for RTL-based designs"**
Student: *D. Paletti*, Politecnico di Milano

2020 **"A Domain-Specific Architecture for Regular Expression"**
2019 Student: *D. Parravicini*, Politecnico di Milano
Co-Supervisor: *C. Pilato, E. Del Sozzo*

2019 **"KMP String matching via FPGA"**
Student: *N. Picca*, Politecnico di Milano

2018 **"A Vectorized Range Unit for Regular Expression DSA"**
Student: *F. Carloni*, Politecnico di Milano

RESEARCH TOOLS

CICERO MLIR	MLIR-based compilation flow and novel microarchitecture of Cicero[C2]. https://github.com/necst/cicero_compiler_cpp
ALVEARE	ALVEARE: A Domain-Specific Framework for Regular Expressions [C5] https://github.com/necst/alveare
POCA	POCA: a PYNQ Offloaded Cryptographic Accelerator on Embedded FPGA-based Systems [C9] https://github.com/necst/POCA
QUEKUF	QUEKUF - An Accurate Union Find Decoder for Quantum Error Correction on the Toric Code [C7] https://github.com/necst/QUEKUF
IMFANT	One Automaton To Rule Them All: Beyond Multiple Regular Expressions Execution [C10] https://github.com/necst/iMFAnt
ATHENA	A GPU-based Framework for Biomedical 3D Rigid Image Registration [C11] https://github.com/necst/athena
HEPHAESTUS	Codesigning and Automating 3D Image Registration on Reconfigurable Architectures [J5] https://github.com/necst/hephaestus

NERONE	NERONE : the Fast Way to Efficiently Execute Your Deep Learning Algorithm at the Edge [J6] https://github.com/necst/NERONE
Quantum benchmark.	On the Design and Characterization of Set Packing Problem on Quantum Annealers [C13] https://github.com/necst/quantum_annealer_benchmarking
CICERO on Arduino	Enabling Efficient Regular Expression Matching at the Edge through Domain-Specific Architectures [C16] https://github.com/necst/cicero-on-vidor4000
YARB	YARB: a Methodology to Characterize Regular Expression Matching on Heterogeneous Systems [C17] https://github.com/necst/yarb
FABER FPGA	Faber: a Hardware/Software Toolchain for Image Registration [J7] https://github.com/necst/faber_fpga
MD BENCH.	A Benchmark Suite for characterizing Molecular Dynamics (MD) simulation on commodity platforms [C19] https://github.com/necst/lammps-benchmarks
FPGA-PROG.	A list of ways to design and program the FPGAs according [J8] https://github.com/emanueledelsozzo/awesome-fpga-programming
SENECA	Deploying efficient medical semantic segmentation models on edge devices [C20] https://github.com/necst/seneca
MOVADO	A Black-Box fitness function approx. library [C21] https://github.com/necst/movado
CFP_ZOO	A cloudFPGA project with domain-specific accelerators for the hybrid multi-cloud era. https://github.com/cloudFPGA/cFp_Zoo
FABER GPU	Exploiting heterogeneous architectures for rigid Image Registration [C22]. https://github.com/necst/faber_biocas
CICERO	A domain specific architecture for Regular Expression matching on FPGA [J10]. https://github.com/necst/cicero
DOVADO	A framework for RTL-based Design Space Exploration [C24] https://github.com/necst/dovado
XLNX	A template repository for Xilinx FPGAs designs https://github.com/necst/xlnx-project-template
IRON	A framework for customizable FPGA-based Image Registration accelerators [C25]. https://github.com/necst/iron
BISMO	A bit-serial DSA for few-bits matrix multiplications [J12]. https://github.com/EECS-NTNU/bismo
CHISEL-SDX	A Chisel wrapper for SDAccel integration [C26] https://github.com/necst/sdaccel_chisel_integration

ASSOCIATION AND VOLUNTEER

AVIS	Blood Donor Volunteer since 2017
IEEE	Member (2017)
ACM	Member (2020)
HIPEAC	Affiliated Member (2023)
IEEE	Computer Society (2017)
ACM	SIGARCH Member (2024)
IEEE	CS Technical Community on Computer Architecture
IEEE	Circuits and Systems
IEEE	Women In Enegineering
IEEE	Volunteer as Larson Award Chair
POLIMI	Open-Day Volunteer 23; 17–20
VOLUNTEER	Different local fairs for catering